Claim Amendments

1-30. Canceled.

31. (New) A method of testing a buffer circuit comprising

driving data signals representative of bits from the buffer circuit in response to a clock signal,

latching the driven data signals in the buffer circuit in response to a strobe signal having a delay relative to the clock signal,

generating a first signal in response to detecting that at least one latched data signal fails to represent its corresponding bit of the buffer circuit,

generating a second signal in response to detecting that all latched data signals fail to represent their corresponding bits of the buffer circuit, and

determining that the buffer circuit is operational in response to a strobe window defined by the first signal and the second signal satisfying criteria associated with proper operation.

32. (New) The method of claim 1 further comprising repeatedly adjusting the delay of the strobe signal, driving data signals from the buffer circuit, and latching driven data signals in the buffer circuit until the first signal and the second signal are generated.

33. (New) The method of claim 1 further comprising repeatedly adjusting the delay of the strobe signal, driving data signals from the buffer circuit, and latching driven data signals in the buffer circuit until the first signal and the second signal are generated or the delay of the strobe signal satisfies criteria associated with failed operation.

34. (New) The method of claim 1 further comprising repeatedly adjusting the delay of the strobe signal and the bits driven from the buffer circuit until the first signal and the second signal are generated or the delay of the strobe signal satisfies criteria associated with failed operation.

35. (New) The method of claim 1 wherein the strobe signal operates at a different frequency than the clock signal.

36. (New) The method of claim 1 comprising generating a pass signal in response to a difference between the delay of the strobe signal associated with the first signal and the delay of the strobe signal associated with the second signal being indicative of a proper strobe window.

37. (New) The method of claim 1 comprising generating a fail signal in response to a difference between the delay of the strobe signal associated with the first signal and the delay of the strobe signal associated with the second signal being indicative of an improper strobe window.

38. (New) An integrated circuit comprising

a driver circuit to drive a plurality of bits from a first storage circuit in response to a clock signal,

a second storage circuit to latch the plurality of bits in response to a strobe signal that is delayed relative to the clock signal;

a comparing circuit to generate a first signal in response to detecting that at least one bit of the first storage circuit differs from its corresponding bit of the second storage circuit and to generate a second signal in response to detecting that all bits of the first storage circuit differ from their corresponding bits of the second storage circuit, and

a control circuit to generate a fail signal if the first signal and the second signal are not generated prior to the delay of the strobe signal having a defined relationship to a limit.

39. (New) The integrated circuit of claim 38 wherein

the control circuit is to adjust the delay of the strobe signal, and

the comparing circuit is to generate the first signal and the second signal based upon the adjusted delay of the strobe signal.

40. (New) The integrated circuit of claim 38 wherein

the control circuit is to adjust the delay of the strobe signal and is to adjust the plurality of bits, and

the comparing circuit is to generate the first signal and the second signal based upon the adjusted delay of the strobe signal and the adjusted plurality of bits.

41. (New) The integrated circuit of claim 38 wherein

the driver circuit is to drive the plurality of bits from the first storage circuit at a first frequency in response to the clock signal which has the first frequency, and

a second storage circuit to latch the plurality of bits at the first frequency in response to the strobe signal that has a second frequency that is different than the first frequency.

42. (New) The integrated circuit of claim 38 wherein the control circuit is to generate a pass signal in response to a difference between the delay of the strobe signal associated with the first signal and the delay of the strobe signal associated with the second signal being indicative of a proper strobe window.

43. (New) The integrated circuit of claim 38 wherein the control circuit is to generate a fail signal in response to a difference between the delay of the strobe signal associated with the first signal and the delay of the strobe signal associated with the second signal being indicative of an improper strobe window.

44. (New) A system comprising

an integrated circuit to drive a plurality of bits in response to a clock signal, to latch the plurality of bits in response to a strobe signal that is delayed relative to the clock signal, and to generate a status signal based upon a strobe window defined by a first delay of the strobe signal associated with at least one latched bit differing from its corresponding driven bit and a second delay of the strobe signal associated with all latched bits differing from their corresponding driven bits, and

a tester coupled to the integrated circuit, the tester to determine whether the integrated circuit is operational based upon the status signal.

45. (New) The system of claim 44 wherein the integrated circuit is to adjust the delay of the strobe signal, is to detect based upon the adjusted delay of the strobe signal whether at least one latched bit differing from its corresponding driven bit and whether all latched bits differ from their corresponding driven bits.

46. (New) The system of claim 44 wherein the integrated circuit is to adjust the delay of the strobe signal, is to adjust the plurality of bits, and is to detect based upon the adjusted delay of the strobe signal and the adjusted plurality of bits whether at least one latched bit differing from its corresponding driven bit and whether all latched bits differ from their corresponding driven bits.

47. (New) The system of claim 44 wherein integrated circuit is to generate the status signal to indicate a pass status in response to a difference between the delay of the strobe signal associated with at least one latched bit differing from its corresponding driven bit and the delay of the strobe signal associated with all latched bits differ from their corresponding driven bits being indicative of a proper strobe window.

48. (New) The system of claim 44 wherein integrated circuit is to generate the status signal to indicate a fail status in response to a difference between the delay of the strobe signal associated with at least one latched bit differing from its corresponding driven bit and the delay of the strobe signal associated with all latched bits differ from their corresponding driven bits being indicative of an improper strobe window.